CLAIMS

What is claimed is:

1. A circuit, comprising:

a first transistor coupled across a first capacitor included in a series of stacked capacitors; and

a second transistor coupled across a second capacitor included in the series stacked capacitors, the first transistor coupled to the second transistor, the first capacitor coupled to the second capacitor, wherein the first and second transistors are adapted to provide a bleed current to the series of stacked capacitors to balance a leakage current imbalance in the series of stacked capacitors.

2. The circuit of claim 1 further comprising a resistor divider network coupled to respective control terminals of the first and second transistors to define an input reference for the circuit.

3. The circuit of claim 2 wherein the resistor divider network comprises at least two resistors coupled to the respective control terminals of the first and second transistors.

4. The circuit of claim 1 wherein the first and second transistors are coupled to a connection point between the first and second capacitors of the series

of stacked capacitors, the first and second transistors adapted to maintain a voltage at the connection point within an input reference range.

5. The circuit of claim 1 wherein the bleed current is substantially equal to the leakage current imbalance in the series of stacked capacitors.

6. The circuit of claim 1 wherein the bleed current is substantially equal to zero when a voltage at the connection point remains fixed at a voltage within an input reference range.

7. The circuit of claim 1 wherein the first and second transistors are coupled in a sink-source follower circuit configuration.

8. The circuit of claim 7 wherein the sink-source follower circuit is coupled to receive an input reference that is a fraction of a voltage applied across the series of stacked capacitors.

9. The circuit of claim 8 wherein the input reference is a range of voltages including upper and lower reference voltages, each of which is offset from the fraction of the voltage applied across the series of stacked capacitors.

10. The circuit of claim 9 wherein the offset of the upper and lower reference voltages from the fraction of the voltage applied across the series of stacked capacitors is zero.

11. The circuit of claim 7 wherein the first and second transistors comprise bipolar junction transistors.

12. The circuit of claim 11 wherein the first and second transistors comprise a PNP transistor and an NPN transistor.

13. The circuit of claim 12 further comprising a first resistor coupled to a collector of the first transistor to limit the bleed current through the first transistor, the circuit further comprising a second resistor coupled to a collector of the second transistor to limit the bleed current through the second transistor.

14. The circuit of claim 1 wherein the circuit is an active circuit included in a power supply circuit.

15. A method, comprising:

providing a bleed current through a first transistor to a connection point between first and second capacitors included in a series of stacked capacitors if a voltage at the connection point rises above an upper reference voltage; and

providing the bleed current through a second transistor to the connection point if the voltage at the connection point falls below a lower reference voltage.

16. The method of claim 15 wherein the voltage at the connection point rises above the upper reference voltage as a result of a leakage current imbalance in the series of stacked capacitors, the method further comprising balancing the leakage current imbalance with the bleed current.

17. The method of claim 16 wherein the bleed current is substantially equal to a difference in leakage currents between the first and second capacitors.

18. The method of claim 15 wherein the voltage at the connection point falls below the upper reference voltage as a result of a leakage current imbalance in the series of stacked capacitors, the method further comprising balancing the leakage current imbalance with the bleed current.

19. The method of claim 18 wherein the bleed current is substantially equal to a difference in leakage currents between the first and second capacitors.

20. The method of claim 15 further comprising maintaining the voltage at the connection point within an input reference voltage range defined by the upper and lower reference voltages.

21. The method of claim 20 wherein an offset between the upper and lower reference voltages is substantially zero.

22. The method of claim 15 further comprising smoothing an output voltage of a diode bridge of a power supply with the series of stacked capacitors.

23. The method of claim 15 further comprising switching off the first and second transistors if the voltage at the connection point is between the upper and lower reference voltages.

24. A circuit, comprising:

a series of stacked capacitors including first and second capacitors coupled across a power supply input;

a first transistor coupled across the first capacitor, the first transistor having a control terminal coupled to receive a first reference voltage; and

a second transistor coupled across the second capacitor, the second transistor have a control terminal coupled to receive a second reference voltage; the first and second capacitors coupled to the series of stacked capacitors at a connection point between the first and second capacitors, the first and second transistors adapted to provide a bleed current to balance a leakage current imbalance in the series of stacked capacitors.

25. The circuit of claim 24 further comprising:

a first resistor coupled to the first transistor to limit the bleed current through the first transistor; and

a second resistor coupled to the second transistor to limit the bleed current through the second transistor.

26. The circuit of claim 24 further comprising a resistor network coupled to the first and second transistors to provide the first and second reference voltages.

27. The circuit of claim 26 wherein the first and second reference voltages provided by the resistor network are different from one another.

28. The circuit of claim 26 wherein the first and second reference voltages provided by the resistor network are the same.